

CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). An electronic component with shielding against stray electromagnetic fields, the electronic component comprising:

a ground potential terminal for receiving an external ground potential;

a semiconductor chip having a semiconductor substrate with an active upper side and a passive rear side having a surface area;

at least one ground lead disposed within said semiconductor substrate and having at least one contact area contacting said upper side of said semiconductor substrate for connecting to said ground potential terminal; and

a continuous electrically conductive buried layer having a surface area corresponding in size to said surface area of said passive rear side and entirely extending over said surface area, said buried layer disposed within said

semiconductor substrate adjacent said passive rear side and connected to said ground potential terminal through said ground lead for providing a rear side shielding with said buried layer, and said buried layer being formed of a semiconductor material doped with an impurity concentration of over  $1 \times 10^{20} \text{ cm}^{-3}$ .

Claim 2 (canceled).

Claim 3 (currently amended). The electronic component according to claim 2 1, wherein said semiconductor material is identical to a material forming said semiconductor substrate.

Claim 4 (original). The electronic component according to claim 1, wherein said semiconductor substrate is formed of monocrystalline silicon.

Claim 5 (original). The electronic component according to claim 1, including an electrically conductive annular layer extending from said upper side of said semiconductor substrate to said buried layer, and disposed in an edge region of said semiconductor chip.

Claim 6 (original). The electronic component according to claim 5, wherein said electrically conductive annular layer is formed of a semiconductor material doped with an impurity concentration of over  $1 \times 10^{20}$  cm<sup>-3</sup>.

Claim 7 (original). The electronic component according to claim 1, wherein the electronic component is a component of a flip-chip mounting technique.

Claim 8 (original). The electronic component according to claim 1, wherein the electronic component is a radio-frequency component.

Claim 9 (currently amended). The electronic component according to claim 1, including solder formations selected from the group consisting of solder balls and solder contact bumps disposed on said contact area, and a shielding ground-carrying line connected to said solder formations.

Claim 10 (original). The electronic component according to claim 9, including a mounting device selected from the group consisting of a printed circuit board and a ceramic substrate, and said solder formations mounted to said mounting device.

Claim 11 (original). The electronic component according to claim 5, including:

output contact areas;

a wiring foil with connecting lines disposed on said upper side of said semiconductor substrate, said contact area of said semiconductor chip is one of a plurality of contact areas and said connecting lines of said wiring foil connecting said contact area of said semiconductor chip to said output contact areas distributed on said wiring foil; and

solder formation selected from the group consisting of solder balls and solder contact bumps disposed on said output contact areas.

Claim 12 (original). The electronic component according to claim 11, wherein said ground potential terminal is connected through at least one of said solder formations, through said wiring foil and through said annular layer to said buried layer.

Claim 13 (withdrawn). A method for producing electronic components with shielding, which comprises the steps of:

providing a semiconductor wafer functioning as a semiconductor substrate formed of a semiconductor material and having an active upper side for at least one integrated circuit for each of the electronics components and a passive rear side;

implanting impurities from the passive rear side of the semiconductor wafer for forming a buried layer being electrically conductive and having a surface area corresponding in size to a surface area of the passive rear side of the semiconductor substrate;

introducing an electrically conductive annular layer for each of the electronic components from the active upper side of the semiconductor wafer as far as the buried layer in an edge region of the integrated circuit;

producing the integrated circuit within the electrically conductive annular layer for each of the electronic components in the semiconductor substrate defining a semiconductor chip for each of the electronic components; and

packaging the semiconductor chip to form the electronic components with the shielding.

Claim 14 (withdrawn). The method according to claim 13, which comprises doping the semiconductor material with an impurity concentration of at least  $1 \times 10^{20} \text{ cm}^{-3}$  for producing the buried layer.

Claim 15 (withdrawn). The method according to claim 14, which comprises forming and soldering solder formations selected from the group consisting of solder balls and solder contact bumps onto contact areas on the active upper side of the semiconductor wafer.

Claim 16 (withdrawn). The method according to claim 15, which comprises connecting the solder formations to a support selected from the group consisting of a printed-circuit board and a ceramic substrate, and connecting at the same time at least one of the solder formations to a ground potential terminal.

Claim 17 (withdrawn). The method according to claim 15, which comprises connecting the contact areas to connecting lines of a wiring foil having further solder formations

selected from the group consisting of solder balls and solder contact bumps.

Claim 18 (withdrawn). The method according to claim 17, which comprises connecting the further solder formations of the wiring foil to lines of a support selected from the group consisting of a printed-circuit board and of a ceramic substrate, at least one of the further solder formations being connected to a ground-carrying line of the support.

Claim 19 (withdrawn). The method according to claim 13, which comprises disposing an annular contact area, which establishes electrical contact with the electrically conductive annular layer, in an edge region of the upper side of the semiconductor chip.

Claim 20 (withdrawn). The method according to claim 18, which comprises electrically connecting one of a number of annularly disposed solder balls and a number of annularly disposed solder contact bumps to the electrically conductive annular layer in an edge region of the individual semiconductor chip.

Claim 21 (withdrawn). A method for producing electronic components with shielding, which comprises the following steps:

providing a semiconductor wafer functioning as a semiconductor substrate having an active upper side for at least one integrated component for each of the electronic components and a passive rear side;

growing an electrically conductive layer formed of an electrically conductive semiconductor material and thereafter an electrically intrinsically conductive layer formed of an electrically intrinsic conductive semiconductor material on the active upper side of the semiconductor wafer by epitaxial growth, the electrically conductive layer becoming a buried layer adjacent the electrically intrinsically conductive layer;

introducing an electrically conductive annular layer for each of the electronic components from the active upper side of the semiconductor wafer, the electrically conductive annular layer extending through the electrically intrinsically conductive layer as far as the buried layer, the electrically conductive annular layer disposed in an edge region of the semiconductor substrate;

producing the integrated circuit within the electrically conductive annular layer for each of the electronic components in the semiconductor substrate defining a semiconductor chip; and

packaging the individual conductor chips to form the electronic components with the shielding.

Claim 22 (withdrawn). The method according to claim 21, which comprises doping the semiconductor material with an impurity concentration of at least  $1 \times 10^{20}$  cm<sup>-3</sup> for forming the buried layer.

Claim 23 (withdrawn). The method according to claim 22, which comprises forming and soldering solder formations selected from the group consisting of solder balls and solder contact bumps onto contact areas on the active upper side of the semiconductor wafer.

Claim 24 (withdrawn). The method according to claim 23, which comprises connecting the solder formations to a support selected from the group consisting of a printed-circuit board and a ceramic substrate, and connecting at the same time at

least one of the solder formations to a ground potential terminal.

Claim 25 (withdrawn). The method according to claim 23, which comprises connecting the contact areas to connecting lines of a wiring foil, the wiring foil having further solder formations selected from the group consisting of solder balls and solder contact bumps.

Claim 26 (withdrawn). The method according to claim 25, which comprises connecting the further solder formations of the wiring foil to lines of a support selected from the group consisting of a printed-circuit board and of a ceramic substrate, at least one of the further solder formations being connected to a ground-carrying line of the support.

Claim 27 (withdrawn). The method according to claim 21, which comprises disposing an annular contact area, which establishes electrical contact for the electrically conductive annular layer, in an edge region of the upper side of the semiconductor chip.

Claim 28 (withdrawn). The method according to claim 26, which comprises electrically connecting one of a number of annularly disposed solder balls and a number of annularly

disposed solder contact bumps to the electrically conductive annular layer in an edge region of the semiconductor chip.

Claim 29 (new). The electronic component according to claim 1, including a shielding ground-carrying line connected to said at least one contact area.